Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application.

Listing of Claims:

1. (currently amended): A memory system comprising:

at least one single in-line memory module (SIMM) including at least one memory device and a signal transmission line connected between the memory device and a connection terminal; [[and]]

at least one dual in-line memory module (DIMM) including at least two memory devices and a signal transmission line connected between the two memory devices and a connection terminal,

a first socket which receives the connection terminal of the at least one SIMM;

a second socket which receives the connection terminal of the at least one DIMM; and

a signal transmission line connected between the first and second sockets,

wherein a length of the signal transmission line of the at least one SIMM is longer than a length of the signal transmission line of the at least one DIMM, and wherein the longer length of the signal transmission line of the at least one SIMM increases the signal delay time of the at least one SIMM to further compensate for the signal delay time difference caused by the signal transmission line connected between the first and second sockets.

2. (currently amended): The memory system according to claim 1, wherein a load of the at least one memory device of the at least one SIMM is less than a load of the memory devices of the at least one DIMM, and wherein

the longer length of the signal transmission line of the at least one SIMM increases a signal delay time of the at least one SIMM to further compensate for the different loads of the at least one memory device of the at least one SIMM and the memory devices of the at least one DIMM.

3. (cancelled)

4. (currently amended): A memory system comprising:

a memory controller;

a first memory module including at least one first memory device having a first load and a first signal transmission line connected between the at least one first memory device and a connection terminal;

a second memory module including at least one second memory device having a second load and a second signal transmission line connected between the at least one second memory device and a connection terminal, wherein the second load is greater than the first load; and

first and second sockets which are connected to the memory controller and which respectively receive the connection terminals of the first and second memory modules,

wherein a length of the first signal transmission line of the first memory module is longer than a length of the second signal transmission line of the second memory module, and wherein the longer length of the first signal transmission line of the first memory module increases a signal delay time of the first memory module to compensate for the different loads of the first and second modules.

5. (cancelled)

6. (currently amended): The memory system according to claim [[5]] 4, further comprising a third signal transmission line connected between the memory controller and the first socket, and a fourth signal transmission line connected between the first socket and the second socket, wherein the longer length of the first signal transmission line of the first memory module further compensates for the signal delay time difference caused by the fourth signal transmission line connected between the first and second sockets.

7. (original): The memory system according to claim 6, wherein each of the first, second and third signal transmission lines includes an impedance matching resistive element.

8. (original): The memory system according to claim 4, wherein the first memory module is a single in-line memory module, and the second memory module is a dual in-line memory module.

9. (currently amended): The memory system according to claim [5]] 4, wherein the first memory module is a single in-line memory module, and the second memory module is a dual in-line memory module.

10. (original): The memory system according to claim 6, wherein the first memory module is a single in-line memory module, and the second memory module is a dual in-line memory module.

11. (original): The memory system according to claim 7, wherein the first memory module is a single in-line memory module, and the second memory module is a dual in-line memory module.